REMARKS

These Amendments are made and filed concurrently with Applicant's Request for Continued Examination. Amendments were made and submitted with the previously filed After Final Amendment, filed August 20, 2007. However, in order to ensure that the record is clear, those amendments are repeated herein along with additional amendments and arguments. Applicants submit the enclosed amendments and arguments as the present state of the application for examination pursuant to the Request for Continued Examination.

Claims 1-6, 9, 10, 26-29, 34, and 35 are pending in the Application. Claims 7-8, 11-25, and 30-33 have been cancelled without prejudice. Claims 1 and 26 are currently amended. Claims 1 and 26 are the independent claims.

Objection to the Title:

The Office Action posed an objection to the title as not descriptive. While Applicants do not admit that the title was not descriptive, they have amended the title in the interest of furthering prosecution of this Application. Applicants respectfully submit that the amended title is accurately descriptive and accordingly respectfully request that the objection be withdrawn.

Claims Rejection under 35 U.S.C. 112, first paragraph:

Regarding Claims 26-29 and 35:

Claims 26-19 and 35 were rejected under 35 U.S.C. 112, first paragraph as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Further, in the Advisory Action, dated December 7, 2007, Claims 26-29 and 35 are continued to be rejected under 35 U.S.C. 112, first paragraph, stating:

> Applicant argues that the claimed TFT array substrate is disclosed at least in the Specification, page 6 line 17 through page 7, line 6. The argument is not persuasive because, nowhere in the specification, including pages 6-7, does the Applicant describe wherein the "mask material dropped onto a semiconductor film" and the conductor layer that "has a portion formed by dropping a droplet," are different features. However, claim 26 recites the mask material and the conductor layer as two different features, and there is no such description, in the specification, of these limitations as two different features.

See, Advisory Action, page 2. Applicants respectfully traverse there rejections.

Specifically, independent Claim 26 was rejected for the following limitation: "a semiconductor layer that has been etched after a mask material is dropped onto a semiconductor film and a conductor layer are formed on the gate electrode." At the suggestion of the Examiner, discussed below, Claim 26 is currently amended to include commas to help clarify the language, and the cited limitation now reads as follows: "a semiconductor layer, that has been etched after a mask material is dropped onto a semiconductor film and a conductor layer, is formed on the gate electrode." The grounds for the rejection posit as follows: "the mask material and the conductor layer are claimed as two different features, and there is no such description in the specification supporting these claimed limitations as two different features." See, Final Office Action, page 3.

Although Applicants traverse the rejection, they recognize from the Examiner's interpretation that the claim could be improved by a clarifying amendment. Initially, Applicants note that the claimed thin film transistor is taught in the elected Embodiment 5, in Figures 39(a) through 43(c). These figures, and the accompanying specification, teach a thin film transistor including a semiconductor film under a conductor forming layer 123 which acts as a mask material when the semiconductor film is etched and processed to form the semiconductor layer 16. Applicants also note that the conductor forming layer 123 serves as the mask layer for formation of the shape of the etched semiconductor layer and, after the processing, the dropped conductor forming layer 123 becomes the conductor layer 122. As disclosed in the specification, the method of manufacturing the thin film transistor will help explain the terminology used to define the device, as follows:

> A TFT [thin film transistor] array substrate according to the present invention includes: a thin film transistor section in which a gate electrode is formed on a substrate, and a semiconductor layer and a conductor layer are formed on the gate electrode via a gate insulation layer, wherein: the conductor layer is formed in contact with the semiconductor layer and one or source and drain electrodes of the thin film transistor section, and has a portion formed by dropping a droplet, the conductor layer and the semiconductor layer having substantially the same shape in the portion formed by dropping a droplet.
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> In this arrangement, a conductor forming layer is formed on a deposited *semiconductor **film*** by dropping a droplet of a conductive material, and the *semiconductor **layer*** is formed by using this conductor forming layer having the shape of the droplet (normally a circular shape) as a mask.

See, Disclosure, page 113, lines 6-20, emphasis added. This structure of this same thin film transistor may also be understood by one of ordinary skill in the art as described through the manufacturing process, which admittedly was not elected for this application, but which is part of the original disclosure. The disclosure states, as follows:

> A TFT array substrate according to the present invention includes: a thin film transistor section in which a gate electrode is formed on a substrate, and a semiconductor layer and a conductor layer are formed on the gate electrode via a gate insulation layer, wherein: the conductor layer is formed in contact with the semiconductor layer and one of source and drain electrodes of the thin film transistor section, and has a portion formed by dropping a droplet, the conductor layer and the semiconductor layer having substantially the same shape in the portion formed by dropping a droplet.
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> In this arrangement, a conductor forming layer is formed on a deposited semiconductor film by dropping a droplet of a conductive material, and the semiconductor layer is formed by using this conductor forming layer having the shape of the droplet (normally a circular shape). The conductor forming layer is then processed to be completed as a conductor layer. This conductor forming layer is used as a mask for forming the semiconductor layer, but is not required to be removed unlike the resist layer; therefore, the removal process can be omitted.

See, Disclosure, page 9, line 22 through page 10, line 16, emphasis added.

Applicants additionally note that the semiconductor layer and the conductor layer as specified in Claim 26 are required to have "substantially the same shape in the portion

formed by dropping a droplet." See, Claim 26. There is no limitation claimed that the device of Claim 26 be manufactured in this manner. It is emphasized that the TFT array substrate specified in Claim 26 may have been created by the use of the conductor forming material dropped on the semiconductor forming layer and then used as a mask, as one generation method, or may have been created by dropping a mask of some other resist material which would later be removed, or by other methods of generation. Therefore the contents of the mask material are not specified in the claim, because they are irrelevant to the resultant specified configuration of the conductor layer and the semiconductor layer.

In order to clarify Claim 26, it is amended to read as follows, in relevant part: "a thin film transistor section in which a gate electrode is formed on a substrate, and in which a semiconductor layer, that has been etched after a mask material is dropped onto a semiconductor film, and a conductor layer are formed on the gate electrode via a gate insulation layer . . .." See, Claim 26, above, as currently amended.

Accordingly, Applicants respectfully request that the rejection be withdrawn. Claims 27-29 and 35 were rejected under the same grounds by virtue of their dependency from Claim 26, and Applicants respectfully request that the rejection as to those claims also be withdrawn.

Claims Rejection under 35 U.S.C. 112, second paragraph:

As a result of an election requirement, the Applicants elected Group I, species embodiment 5, comprising Claims 1-10, 26-29, 34, and 35 as disclosed in Figures 39-43, and in the Disclosure beginning at page 80.

Regarding Claims 1, 2-6, 9, 10, and 34:

Claims 1, 2-6, 9, 10, and 34 were rejected under 35 U.S.C. 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Specifically, independent Claim 1 is cited as unclear and ambiguous in reciting, in relevant part: "a semiconductor layer that has been etched after a mask material is dropped on a semiconductor film." The Office action interprets the claim element of "a semiconductor film" as being the same element as "the semiconductor layer," and states that they are interpreted for examination as the same elements. See, Final Office Action, page 3. Based on its interpretation of the claim elements, the Office Action suggests re-casting the phrase as follows: "a semiconductor layer, that has been etched after a mask material is dropped onto the semiconductor layer, is formed on the gate electrode via a gate insulation layer." Applicant appreciates the Examiner's observations and suggestions. However, the claim elements "semiconductor film" and "semiconductor layer" are, in fact, two different elements.

The disclosure specifies a "semiconductor film" as the covering of semiconductor forming material, which, after processing including etching, will become the "semiconductor layer." This transition from the "semiconductor film" to the "semiconductor layer" is taught in the specification according to Claim 1, as follows:

> A manufacturing method of the TFT array substrate according to the present invention includes the steps of: (a) forming a gate electrode on a substrate; (b) forming a gate insulation layer on the gate electrode; (c) depositing a semiconductor film on the gate insulation layer; (d) forming a resist layer having a shape of a droplet by dropping a droplet of a resist material on the semiconductor film; and (e) removing the resist layer, after processing the semiconductor film corresponding to the shape of the resist layer so as to create a semiconductor layer of a thin film transistor section.

See, Disclosure, page 106, lines 12-21, emphasis added.

The Examiner suggested that the claims language of Claim 1 would be more clear with the addition of commas. The Applicants appreciate the suggestion and have amended Claim 1 to add commas to clarify the claimed structure. Applicants note that pursuant to the above discussion of Claim 1, they are very willing to consider any further suggestions from the Examiner to further clarify the claims language.

Accordingly, Applicants respectfully traverse the rejection of Claim 1 under 35 U.S.C. 112, second paragraph on the grounds that "semiconductor film" and "semiconductor layer" are the same element, and respectfully requests that the rejection be withdrawn. Claims 2-6, 9, 10, and 34 were rejected under the same grounds by virtue of their dependency from Claim 1, and Applicants respectfully request that the rejection as to those claims also be withdrawn.

Regarding Claims 26-29 and 35:

Claims 26-19 and 35 were rejected under 35 U.S.C. 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Specifically, independent Claim 26 is cited as unclear and ambiguous for the same reason cited against Claim 1, as discussed above – that the elements "semiconductor film" and "semiconductor layer" were the same element. For the reasons argued above, Applicants respectfully traverse these rejections on the ground that "semiconductor film" and "semiconductor layer" are, in fact, different elements, and further request that the rejection of these claims be withdrawn.

Applicants note that the Examiner also recommended the addition of commas to Claim 26 to help clarify the claim. This recommendation has been well received by the Applicants and Claim 26 is amended to include the commas as suggested by the Examiner. Applicants note that they are very willing to consider any further suggestions from the Examiner to further clarify the claims language.

Claim Rejections under 35 U.S.C. 102/103:

Claims 1-6, 9, 10, and 34 are rejected under either 35 U.S.C 102(e) or 103(a) as either anticipated or obvious over Furusawa (U.S. Patent Application Publication 2003/0219934) [hereinafter "Furusawa"].

Applicants respectfully submit that Furusawa is not a proper prior art reference against the present Application.

The present Application claims priority to two Japanese Patent Applications, JP 2002-365337, filed December 17, 2002, and JP 2002-255538, filed August 30, 2002. Both Japanese patent applications were filed as priority applications to the PCT filing, of which this Application is the U.S. National Phase. The PCT Application was filed August 29, 2003, as PCT/JP03/11057, and designated the United States. The present Application was filed on February 25, 2005, claiming priority pursuant to 35 U.S.C. 371. The U.S. Patent Office acknowledged Applicants' claim for foreign priority at least in the Office Action dated August 20, 2007. Accordingly, the priority date of this Application is August 30, 2002 and December 17, 2002.

Applicants have prepared verified English language translations of their Japanese priority patent applications in order to perfect their claim of foreign priority. These translations were filed in this Application on January 15, 2008.

Applicants respectfully note that Furusawa claims priority to its Japan filing date of April 22, 2002 (JP 2002-119965). Furusawa was filed in the U.S. on April 21, 2003 (Application No. 10/420,540) and the application was published in the U.S. on November 27, 2003 (U.S. Patent Application Publication 2003/0219934 A1). The 102(e) date for Furusawa is the filing date of the U.S. Application, which is April 21, 2003. See, MPEP 706.02(f)(1) II, Example 3. The 102(e) prior art date of Furusawa does not predate either August 30, 2002 or December 17, 2002, which are the priority dates for this Application. Therefore, Applicants respectfully submit that Furusawa is not a prior art reference against the invention of this Application.

Claims 26-29 and 35 are rejected under either 35 U.S.C 102(e) or 103(a) as either anticipated or obvious over Kawase (U.S. Patent 7,198,885) [hereinafter "Kawase"].

Applicants respectfully submit that Kawase is not a proper prior art reference against the present Application.

Applicants note that Kawase claims priority to Great Britain patent application 0211424.7, which was filed May 17, 2002. The Application was filed under PCT as PCT/GB03/02131, on May 19, 2003, designating the US, and published in the English language as WO03/098696, on November 25, 2004. The 102(e) priority date for Kawase is the PCT filing date of May 19, 2003. See, MPEP 706.02(f)(1) II, Example 4. The 102(e) priority date of Kawase is later than the priority dates for this Application of August 30, 2002 and December 17, 2002.

Additionally, Applicants note that the Final Office Action in this Application cites to Figures 7 and 8, and 12, lines 42-59 as the teachings in Kawase that support rejection of Claims 26-29 and 35. See, Office Action, pages 9-11. Figures 7 and 8 do not appear in the PCT publication. They were added by a preliminary amendment to the U.S. Application, which was filed December 24, 2003. See, PAIR, Image File Wrapper of Application 10/482,101, Preliminary Amendment – Drawings (Figures 7 and 8) and Specification (page 12 adding Figures 7 and 8, and pages 19-21, adding the text cited by the Office Action in the present Application). Therefore, the subject matter cited in the Office Action has a priority date no earlier than December 24, 2003. As noted above, the present application has a priority date based on the underlying Japan Patent Applications of August 30, 2002 or December 17, 2002, which is approximately a year before the amendments to Kawase that form the basis of the rejection. Therefore, on additional grounds, Applicants again respectfully submit that Kawase is not a prior art reference against the invention of this Application. The subject matter cited in Kawase in rejection of this Application did not exist prior to the priority filing of this Application.

In summary, Applicants respectfully submit that Furusawa and Kawase are not proper prior art references because their earliest prior art dates do not pre-date the filing of the priority applications for this Application. Applicants further respectfully submit that Kawase is additionally not a proper prior art reference because the subject matter cited against this Application was not added to Kawase until an amendment to the U.S. application, which was made after the priority date of this Application.

Conclusion

Applicant's further respectfully submit that in view of the above amendment, the pending application is in condition for allowance.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Michael R. Cammarata, Reg. No. 39,491 at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37.C.F.R. §§1.16 or 1.17; particularly, extension of time fees.

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Respectfully submitted,

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